REMARKS

Applicant has carefully reviewed and considered the latest communications from the US Patent Office. Applicant respectfully traverses Examiner's rejection and requests reconsideration in view of the argument which follows.

Background

Examiner relies primarily on Guzman-Casillas (United States Patent Number 6,028,754) to reject the independent claims of the present application. In particular, Examiner claims that comparator 72 and timer 66 are part of a filter circuit "which performs the filtering of the signal when CCVT transients are present..." *See* Office Action dated 9/21/06, p.6. Before exploring why the independent claims of the present application are not unpatentable, background information on the definition of "filter" as understood by those of ordinary skill in the art and the workings of the invention disclosed by Guzman-Casillas is appropriate.

The Penguin Dictionary of Electronics defines "filter" as:

> An electrical network that will transmit signals with frequencies within certain designated ranges *(pass bands)* and suppress signals of other frequencies *(attenuation bands)*. The frequencies that separate the pass and attenuation bands are the cut-off frequencies...
>
> E.C. Young, "The Penguin Dictionary of Electronics," p. 195, Second Edition, 1988, Penguin Books USA Inc., New York, New York (emphasis in original).

The Electrical Engineering Handbook gives a similar definition:

> An *electrical filter* is a circuit that is designed to introduce gain or loss over a prescribed range of frequencies.
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> Richard C. Dorf, "The Electrical Engineering Handbook," p. 205, 2nd Edition, 1997, CRC Press, Salem, Massachusetts (emphasis in original).

Both the Penguin Dictionary of Electronics and the Electrical Engineering Handbook are well known treatises within the field of electrical engineering, and would be understood to reflect the understanding of a person of ordinary skill in the art.

Guzman-Casillas discloses a system for calculating a trip signal based on dynamically modifying the reach of a protective relay in response to the detection of a fault. *See* Guzman-Casillas Abstract. A circuit for accomplishing this purpose is disclosed, *see* Guzman-Casillas FIG. 6, and discussed in detail. *See* Guzman-Casillas Col. 5, Line 27 – Col. 9, Line 40.

Elements of the circuit compare the absolute voltage of each phase referenced to ground with a threshold to determine an undervoltage condition. *See* Guzman-Casillas FIG 6, and Col. 6, Lines 22-27. The results of these comparisons are digital binary outputs that are fed into OR gate 42, where they generate signal 27PG. *See* Guzman-Casillas FIG 6, and Col. 6, Lines 25-27. Neither the output of comparator 40 nor the output of OR gate 42 is a filtered version of its input signals.

The circuit comprising of comparator 44 and OR gate 46 is analogous to the circuit comprising comparator 40 and OR gate 42, except that the input signals are phase-to-phase voltages. *See* Guzman-Casillas FIG. 6 and Col. 6, Lines 38-53. Neither the output of comparator 44 nor the output of OR gate 46 is a filtered version of its input signals.

The circuit comprising comparator 50 and OR gate 54 is analogous to the undervoltage detection circuit except that an overcurrent condition referenced to ground is detected. *See* Guzman-Casillas FIG. 6 and Col. 7, Lines 1-27. The circuit comprising comparator 56 and OR gate 58 is similarly analogous to the undervoltage detection circuit except that an overcurrent condition between the different phases are detected. *See* Guzman-Casillas FIG. 6 and Col. 7,

Lines 28-39. None of elements 50, 54, 56, and 58 produce a filtered representation of any of its inputs.

The outputs of OR gates 42 and 54 are fed into AND gate 60 along with signal Z1G. *See* Guzman-Casillas FIG 6 and Col. 7, Lines 40-45. The Z1G signal indicates assertion of the zone 1 phase-to-ground distance element. *See* Guzman-Casillas Col. 6, Lines 35-37. The output of AND gate 61 is a digital binary output, and is not a filtered representation of any of its inputs.

The outputs of AND gates 60 and 61 are fed into OR gate 62. *See* Guzman-Casillas FIG. 6 and Col. 7, Lines 53-55. The output of OR gate 62 is a digital binary output, and is not a filtered representation of any of its inputs.

The output of OR gate 62 is fed into AND gate 64 along with signals SOFTE and SPO+3PO. *See* Guzman-Casillas FIG.6 and Col. 7, Lines 55-57. The SOFTE signal (switch onto fault enable) indicates the re-closing of a previously tripped breaker. *See* Guzman-Casillas Col. 7, Lines 58-60. The SPO+3PO (single pole open OR all 3 poles open) signal indicates when either a single pole is open or when all three poles are open. *See* Guzman-Casillas, Col. 7, Lines 60-65. The output of AND gate 64 is a digital binary output, and is not a filtered representation of any of its inputs.

The output of AND gate 64 is fed into timer 66. *See* Guzman-Casillas FIG. 6 and Col. 7, Lines 65-67. Timer 66 provides a delay element of 1.375 cycles upon detection of a change in its input from 0 to one, which value was selected as typically sufficient to delay the operation of the circuit past the duration of a CCVT transient. *See* Guzman-Casillas Col. 8, Lines 2-4. The output of timer 66 is not a filtered representation of any of its inputs, nor is it a filtered representation of any signal indicating the occurrence of a CCVT transient.

A second leg of the circuit disclosed by Guzman-Casillas calculates a digital representation of the smoothness of the m calculation signal. *See* Guzman-Casillas Lines 4-14. As discussed, the m calculation signal is not filtered in any way by the disclosed circuit; all that is provided is an indication of when the rate of change of the m calculation signal exceeds a calculated value or threshold.

The second leg of the circuit contains a comparator, *see* element 72, generates a digital output (i.e.; either high or low), dependent on the following comparison:

> $-0.15 * mab(k) + 0.135 < |mab(k) - mab(k-1)|$ where mab is the m calculation for phase AB; k is the most recent determination of the such a value, and k-1 is the value immediately previous to the most recent (k) value.
>
> *See* Guzman-Casillas FIG. 6 and Col. 8, Lines 15-21.

Though one of the inputs to the comparator $|mab(k) - mab(k-1)|$ may be considered a filter, the output of the comparator is not a filtered value. The output of comparator is a digital binary output dependent on the result of the referenced comparison, and is therefore a representation of when the rate of change in the m quantity exceeds a calculated threshold. The output of the comparator 72 is not a filtered version of its inputs.

The output of comparator 72 is fed into AND gate 74, along with signal mAB1 to form signal AB. *See* Guzman-Casillas FIG. 6 and Col. 8, Lines 29-44. Signal mAB1 is a digital binary output that results from the comparison of signal mab and a threshold referred to as "ZONE1." *See* Guzman-Casillas FIG. 6 and Col. 8, Lines 44-46. Neither the output of AND gate 74 nor the output of comparator 76 is a filtered version of its input signals.

The output of AND gate 74 is fed into OR gate 78, along with signals BC and CA (which are analogous to signal AB) and signals A, B, and C. *See* Guzman-Casillas FIG. 6, where OR

gate 78 is mislabeled 79, and Col. 8, Lines 51-54. Signals A, B, and C are analogous to signals AB, BC, and CA, but are calculated by comparing the m value with respect to ground for a given phase to a calculated quantity or threshold. *See* Guzman-Casillas FIG. 6 and Col. 8, Lines 55-61. None of signals AB, BC, CA, A, B, or C are filtered versions of any other signal.

The output of OR gate 78 is fed into timer 80. *See* Guzman-Casillas FIG. 6, where timer 80 is mislabeled 30, and Col. 8, Line 62. Timer 80 provides a rising-edge delay element of 3/8 a cycle to the signal generated by OR gate 78. *See* Guzman-Casillas Col. 9, Lines 1-4. The output of timer 80 is not a filtered version of any of its inputs.

The output of timer 66 and the output of timer 80 are fed into AND gate 68. *See* Guzman-Casillas FIG. 6 and Col. 9, Lines 5-10. The output of AND gate 68 is a digital binary output, and is not a filtered version of any of its inputs.

The output of AND gate 68 is fed into AND gate 82 along with signal representing a zone 1 phase or ground assertion from a zone 1 distance element. *See* Guzman-Casillas FIG. 6 and Col. 9, Lines 5-12. The output of this circuit is a fault indication that is tolerant of CCVT transients. *See* Guzman-Casillas Col. 9, Lines 21-30. The disclosed circuit does not provide a filtered version of any of its inputs.

Novelty and Non-Obviousness of the Independent Claims

Claim 1 stands rejected under 35 U.S.C. § 102(b) as anticipated by Guzman-Casillas. However, as explained above, Applicant respectfully disagrees with the proposition that Guzman-Casillas discloses "a filter circuit responsive to said quantity for filtering said quantity..." As Guzman-Casillas does not disclose every element of claim 1, Applicant respectfully contends that Guzman-Casillas cannot anticipate claim 1. Further, as the combined

prior art does not teach or suggest every element of claim 1, claim 1 cannot be obvious in view of the cited prior art. *See* MPEP §706.02(j).

As claims 2,3,5,6 and 7 are dependent on claim 1, if claim 1 is found allowable, claims 2,3,5,6, and 7 should be allowed as well.

Claim 8 stands rejected under 35 U.S.C. §103(a) as unpatentable over Guzman-Casillas. However, as explained above Applicant respectfully disagrees with the proposition that Guzman-Casillas discloses "an apparatus for selecting one of a filtered m value and an unfiltered m value..." As the cited prior art does not teach or suggest every element of claim 8, claim 8 cannot be obvious in view of the cited prior art. *See* MPEP §706.02(j).

As claims 10 and 11 are dependent on claim 8, if claim 8 is found allowable, claims 10 and 11 should be allowed as well.

Claim 14 stands rejected under 35 U.S.C. §103(a)as unpatentable over Guzman-Casillas. However, as explained above, Applicant disagrees with the assertion that Guzman-Casillas discloses "a filter adapted to filter the unfiltered m value to form the filtered m value." As the cited prior art does not teach or suggest every element of claim 14, claim 14 cannot be obvious in view of the cited prior art. *See* MPEP §706.02(j).

As claims 15, 16, and 17 are dependent on claim 14, if claim 14 is found allowable, claims 15-17 should be allowed as well.

CONCLUSION

Accordingly, after review of the previous correspondence along with the further clarifications of this communication, Applicant respectfully submits this application is now in condition for allowance. Applicant therefore requests issuance of a timely notice of allowance. However, should Examiner be of the opinion that further amendment or response is required; Applicant encourages Examiner to contact the undersigned attorney at the attorney at the telephone number set forth below. Further, although no additional fees are believed to be due at this time, the Commissioner is authorized to charge any additional fees or deficiencies or credit any overpayments to Cook, Alex, McFarron, Manzo, Cummings & Mehler, Ltd., Deposit Account No. 50-1039 with reference to attorney docket number (1444-0093).

Respectfully submitted,

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